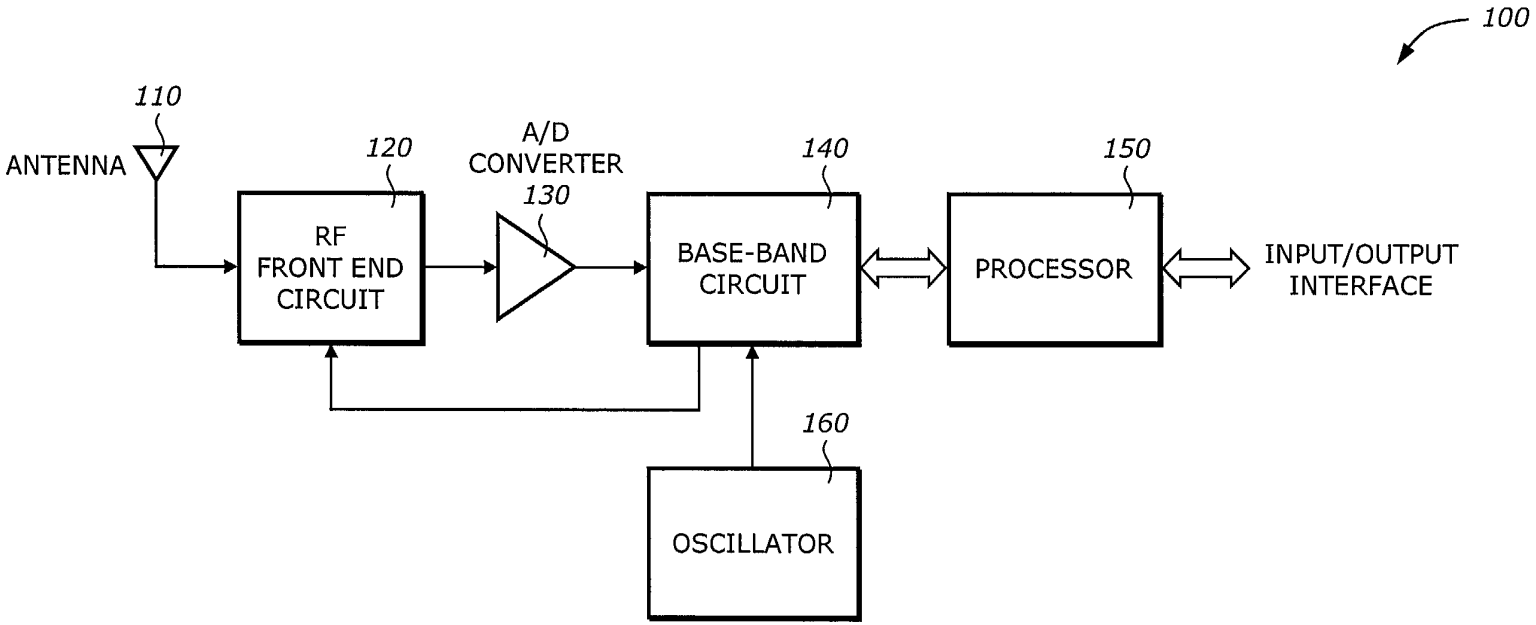
100
110
ANTENNA
120
RF
FRONT END
CIRCUIT
A/D
CONVERTER
130
140
BASE-BAND
CIRCUIT
150
PROCESSOR
INPUT/OUTPUT
INTERFACE
160
OSCILLATOR

FIG. 1

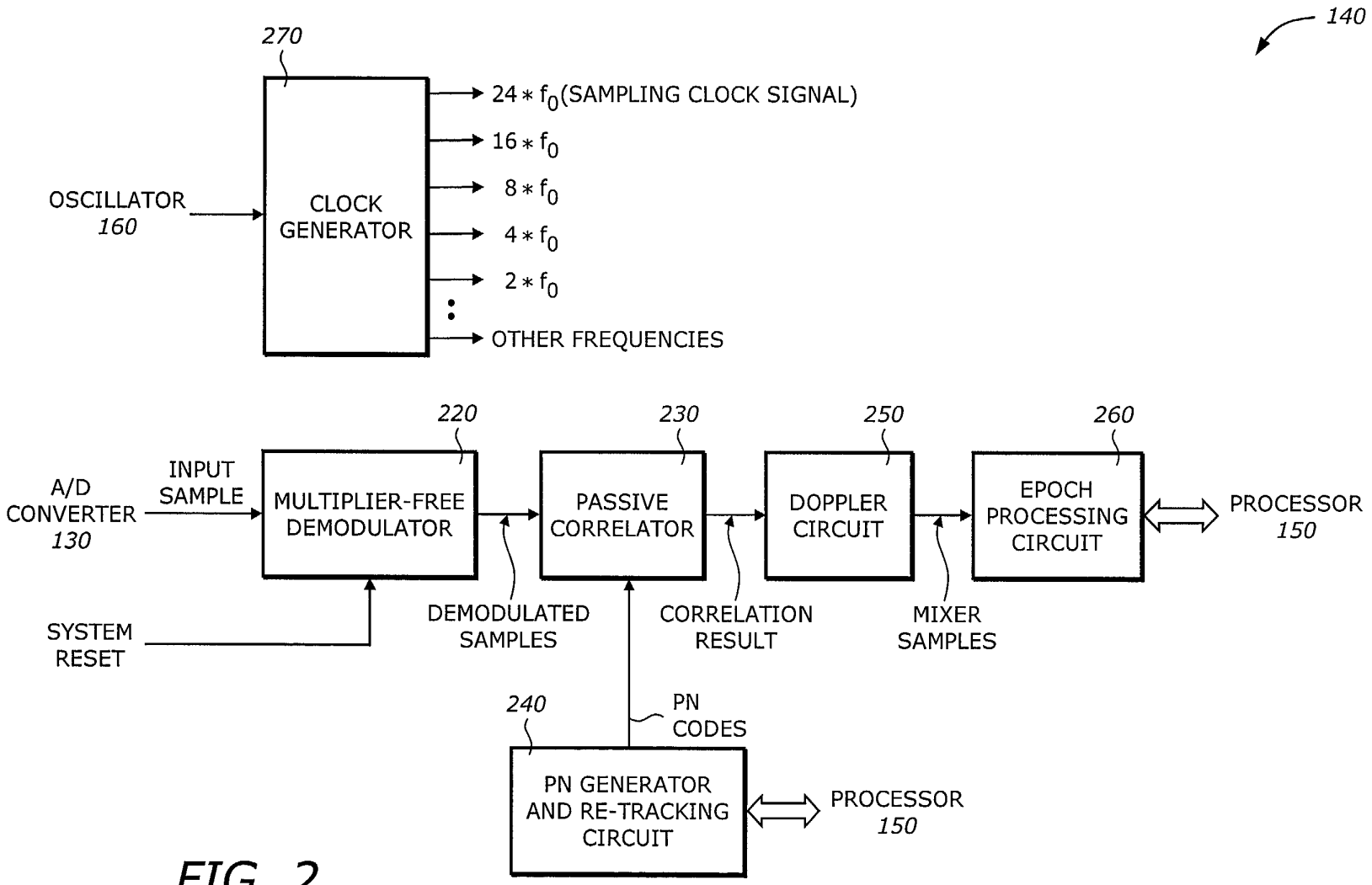
140
270
24 * f0 (SAMPLING CLOCK SIGNAL)
16 * f0
8 * f0
4 * f0
2 * f0
OTHER FREQUENCIES
OSCILLATOR
160
CLOCK GENERATOR
220
230
250
260
A/D CONVERTER
130
INPUT SAMPLE
MULTIPLIER-FREE DEMODULATOR
PASSIVE CORRELATOR
DOPPLER CIRCUIT
EPOCH PROCESSING CIRCUIT
PROCESSOR
150
SYSTEM RESET
DEMODULATED SAMPLES
CORRELATION RESULT
MIXER SAMPLES
240
PN CODES
PN GENERATOR AND RE-TRACKING CIRCUIT
PROCESSOR
150

FIG. 2

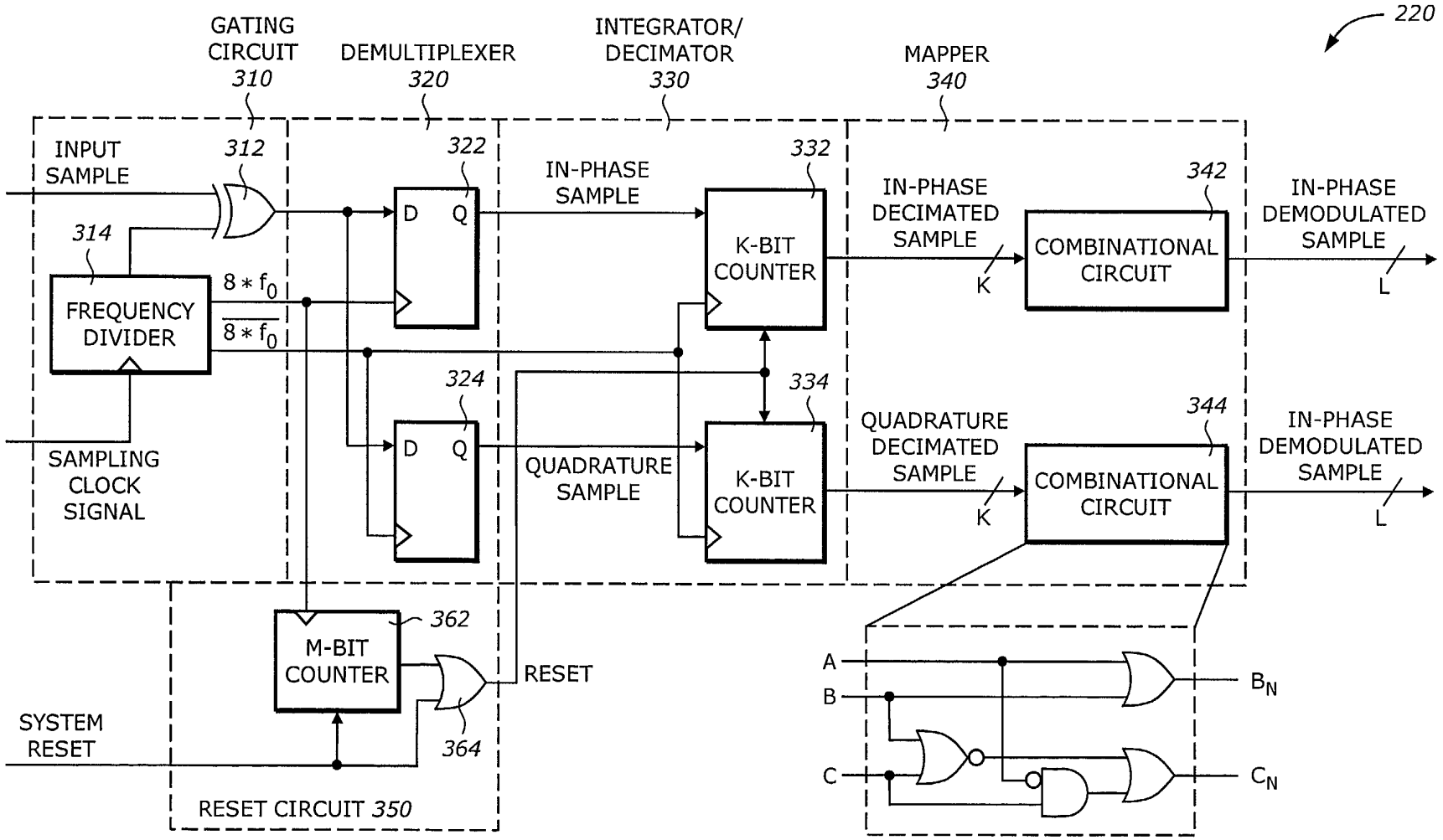
220
GATING CIRCUIT 310
DEMULTIPLEXER 320
INTEGRATOR/ DECIMATOR 330
MAPPER 340
INPUT SAMPLE
312
314
FREQUENCY DIVIDER
8 * f0
8 * f0
SAMPLING CLOCK SIGNAL
322
D Q
324
D Q
IN-PHASE SAMPLE
QUADRATURE SAMPLE
332
K-BIT COUNTER
334
K-BIT COUNTER
IN-PHASE DECIMATED SAMPLE
K
342
COMBINATIONAL CIRCUIT
IN-PHASE DEMODULATED SAMPLE
L
QUADRATURE DECIMATED SAMPLE
K
344
COMBINATIONAL CIRCUIT
IN-PHASE DEMODULATED SAMPLE
L
362
M-BIT COUNTER
RESET
364
SYSTEM RESET
RESET CIRCUIT 350
A
B
C
BN
CN

FIG. 3

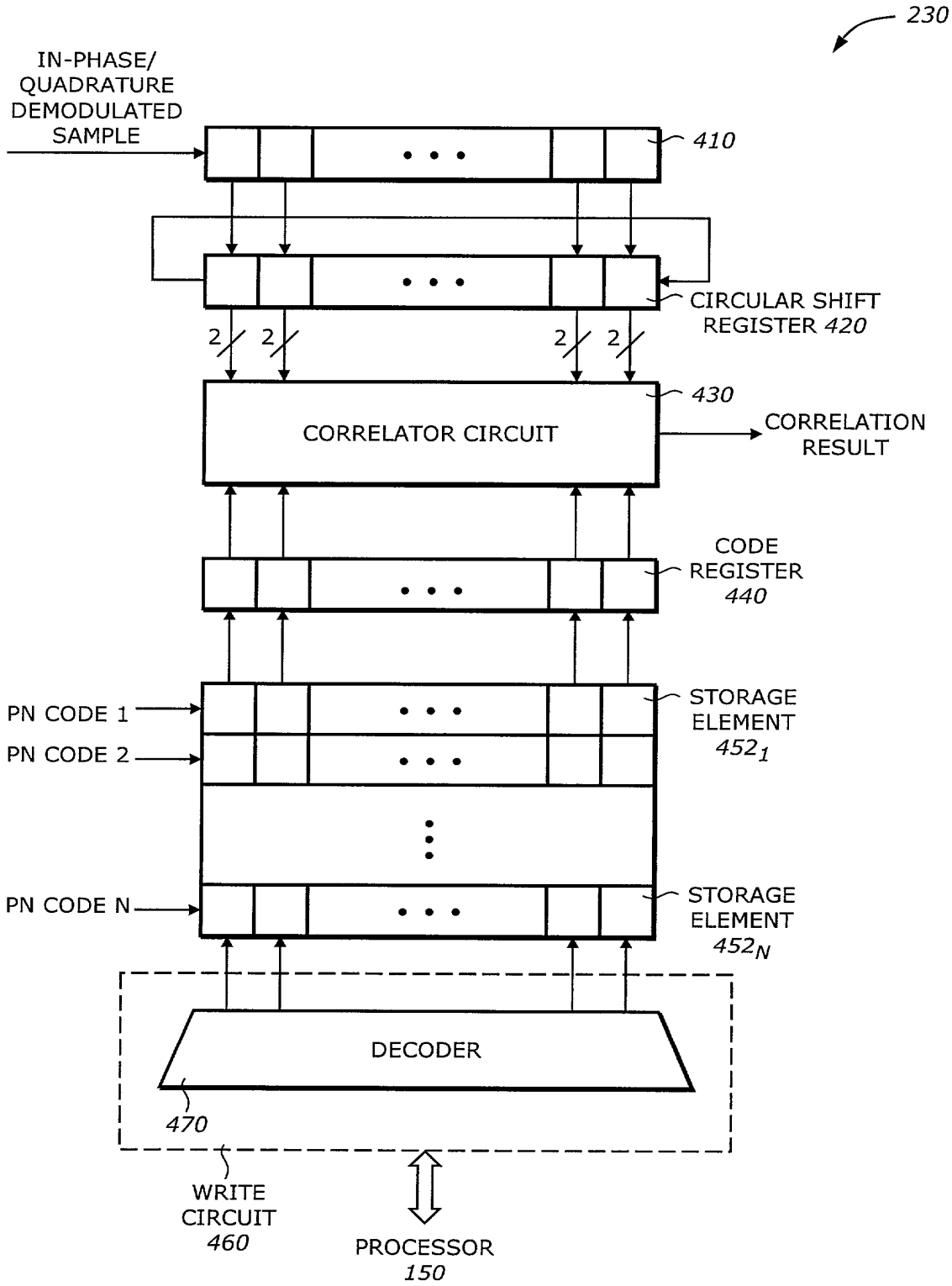
230
IN-PHASE/
QUADRATURE
DEMODULATED
SAMPLE
410
CIRCULAR SHIFT
REGISTER 420
2
2
2
2
430
CORRELATOR CIRCUIT
CORRELATION
RESULT
CODE
REGISTER
440
PN CODE 1
PN CODE 2
PN CODE N
STORAGE
ELEMENT
452_1
STORAGE
ELEMENT
452_N
DECODER
470
WRITE
CIRCUIT
460
PROCESSOR
150

FIG. 4

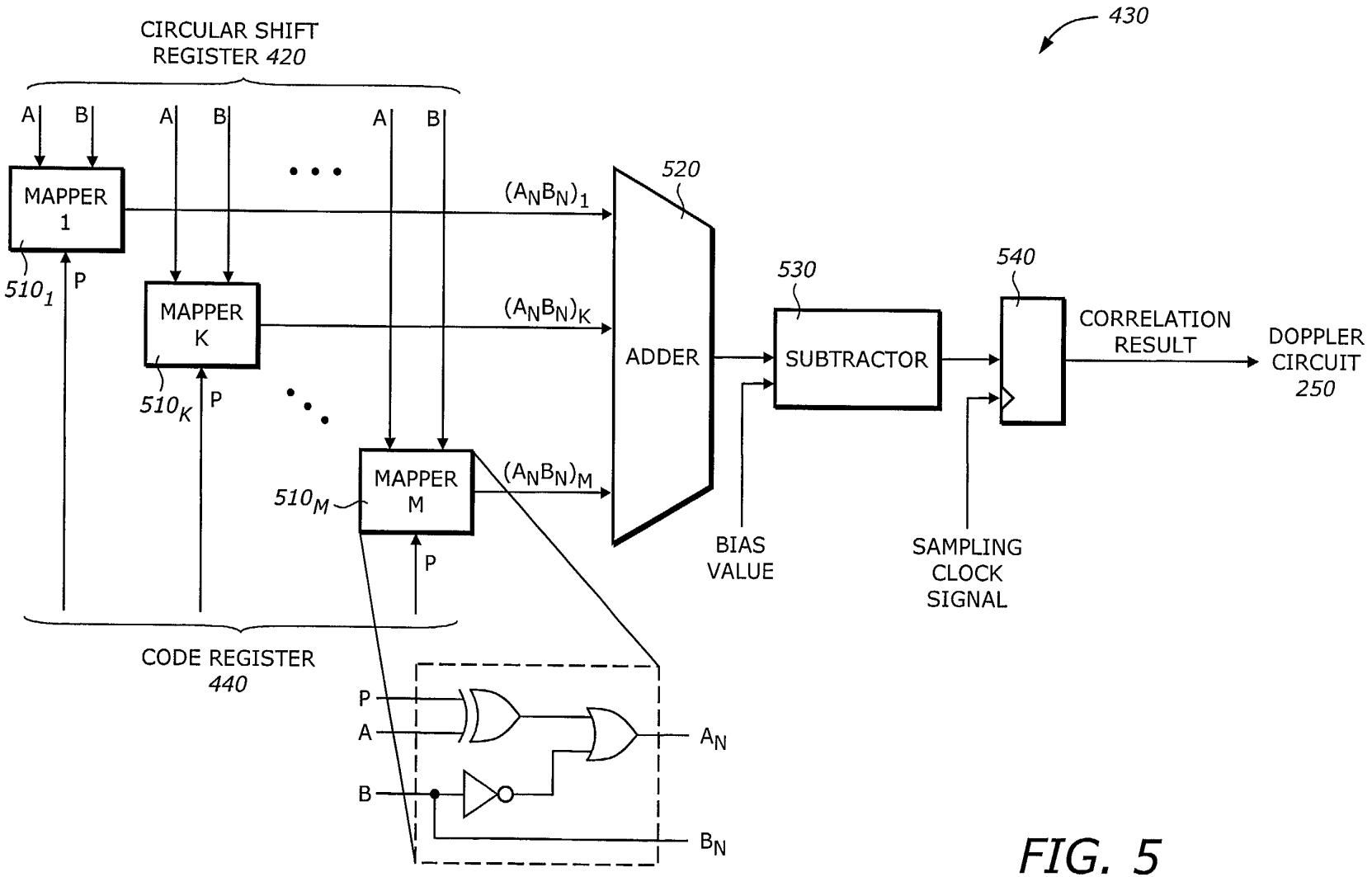
430
CIRCULAR SHIFT REGISTER 420
A
B
MAPPER 1
510_1
P
MAPPER K
510_K
MAPPER M
510_M
$(A_NB_N)_1$
$(A_NB_N)_K$
$(A_NB_N)_M$
520
ADDER
530
SUBTRACTOR
540
CORRELATION RESULT
DOPPLER CIRCUIT 250
BIAS VALUE
SAMPLING CLOCK SIGNAL
CODE REGISTER 440
A
B
A_N
B_N

FIG. 5

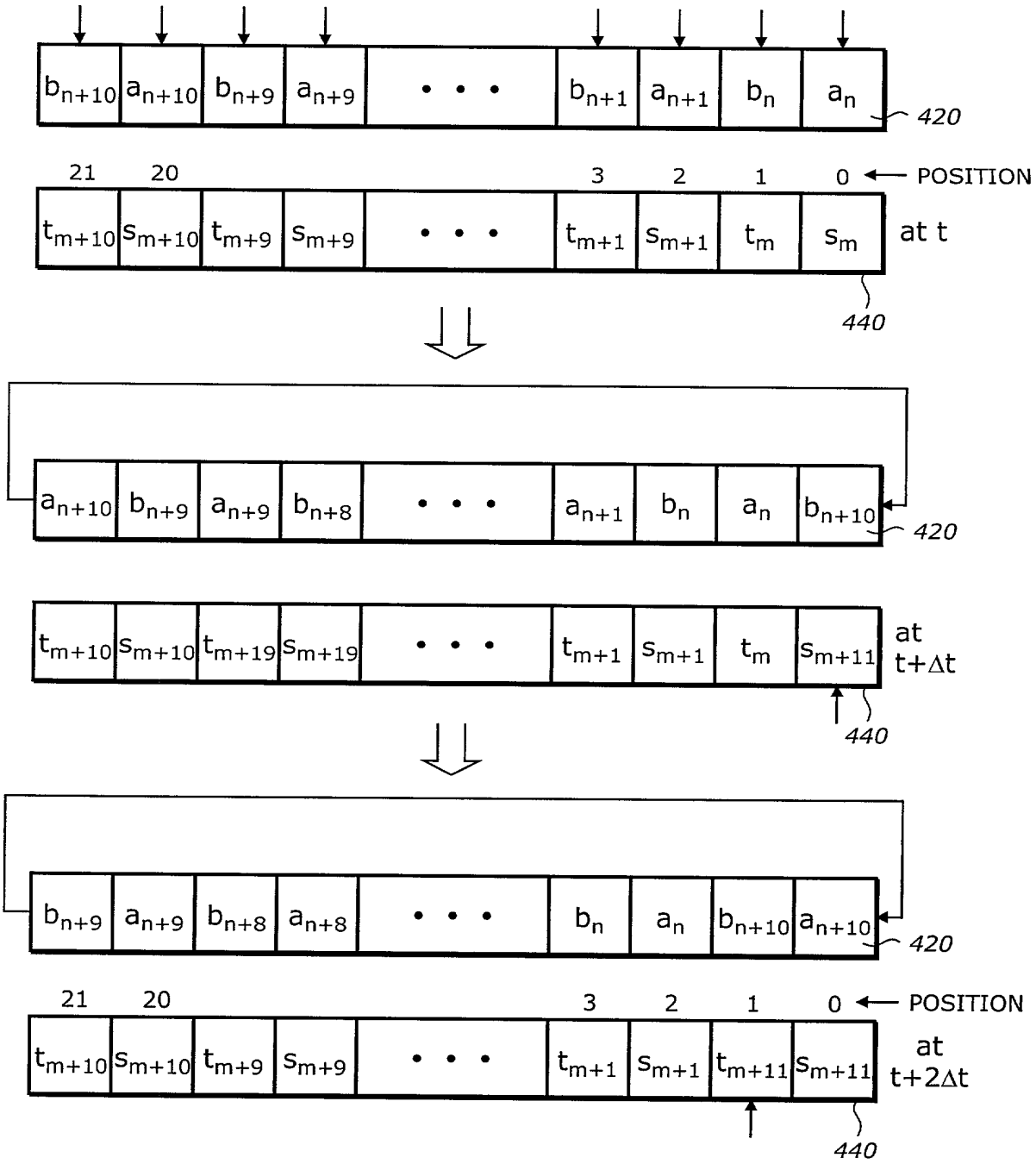
b_{n+10} a_{n+10} b_{n+9} a_{n+9} • • • b_{n+1} a_{n+1} b_n a_n
420
21 20 3 2 1 0 POSITION
t_{m+10} s_{m+10} t_{m+9} s_{m+9} • • • t_{m+1} s_{m+1} t_m s_m
at t
440
a_{n+10} b_{n+9} a_{n+9} b_{n+8} • • • a_{n+1} b_n a_n b_{n+10}
420
t_{m+10} s_{m+10} t_{m+19} s_{m+19} • • • t_{m+1} s_{m+1} t_m s_{m+11}
at
$t+\Delta t$
440
b_{n+9} a_{n+9} b_{n+8} a_{n+8} • • • b_n a_n b_{n+10} a_{n+10}
420
21 20 3 2 1 0 POSITION
t_{m+10} s_{m+10} t_{m+9} s_{m+9} • • • t_{m+1} s_{m+1} t_{m+11} s_{m+11}
at
$t+2\Delta t$
440

FIG. 6

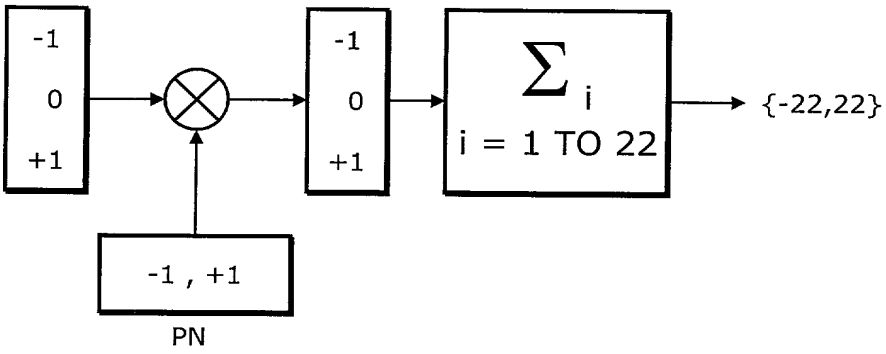

FIG. 7A

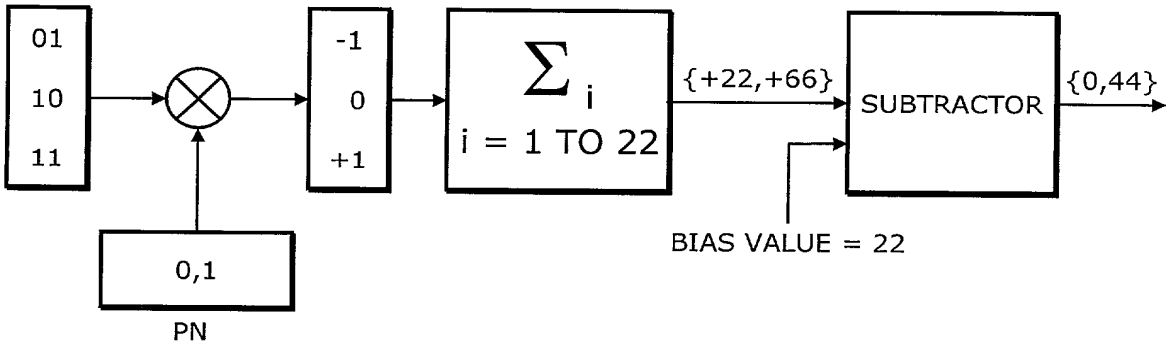

FIG. 7B

PN CODE

DATA SAMPLES	0	1
01	01	11
10	10	10
11	11	01

FIG. 7C

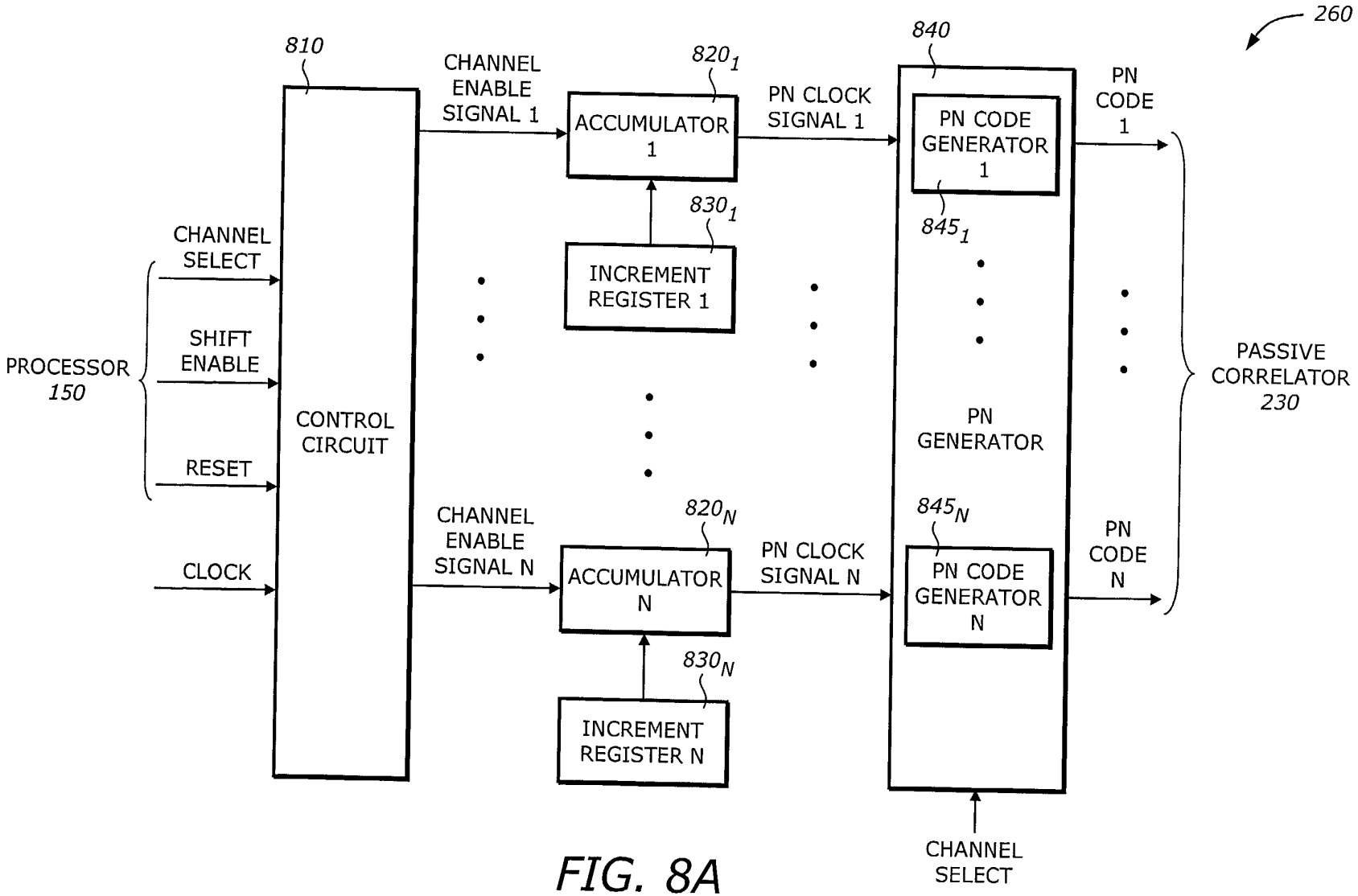
260
810
CHANNEL ENABLE SIGNAL 1
820 1
ACCUMULATOR 1
PN CLOCK SIGNAL 1
840
PN CODE GENERATOR 1
PN CODE 1
830 1
845 1
INCREMENT REGISTER 1
CHANNEL SELECT
SHIFT ENABLE
PROCESSOR 150
RESET
CLOCK
CONTROL CIRCUIT
PN GENERATOR
PASSIVE CORRELATOR 230
CHANNEL ENABLE SIGNAL N
820 N
ACCUMULATOR N
PN CLOCK SIGNAL N
845 N
PN CODE GENERATOR N
PN CODE N
830 N
INCREMENT REGISTER N
CHANNEL SELECT

FIG. 8A

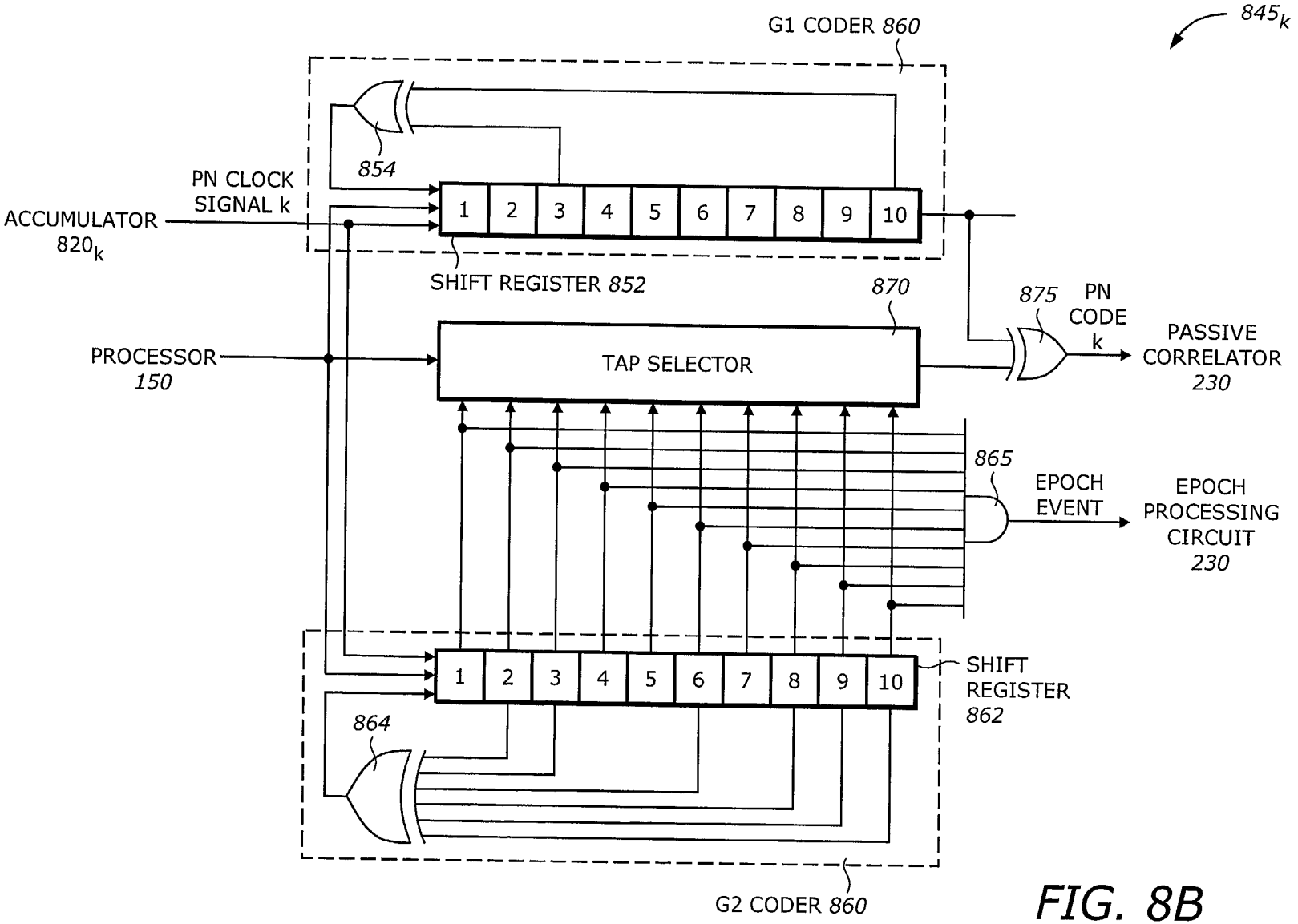
845_k
G1 CODER 860
854
PN CLOCK SIGNAL k
ACCUMULATOR 820_k
1 2 3 4 5 6 7 8 9 10
SHIFT REGISTER 852
870
875
PN CODE k
PROCESSOR 150
TAP SELECTOR
PASSIVE CORRELATOR 230
865
EPOCH EVENT
EPOCH PROCESSING CIRCUIT 230
1 2 3 4 5 6 7 8 9 10
SHIFT REGISTER 862
864
G2 CODER 860

FIG. 8B

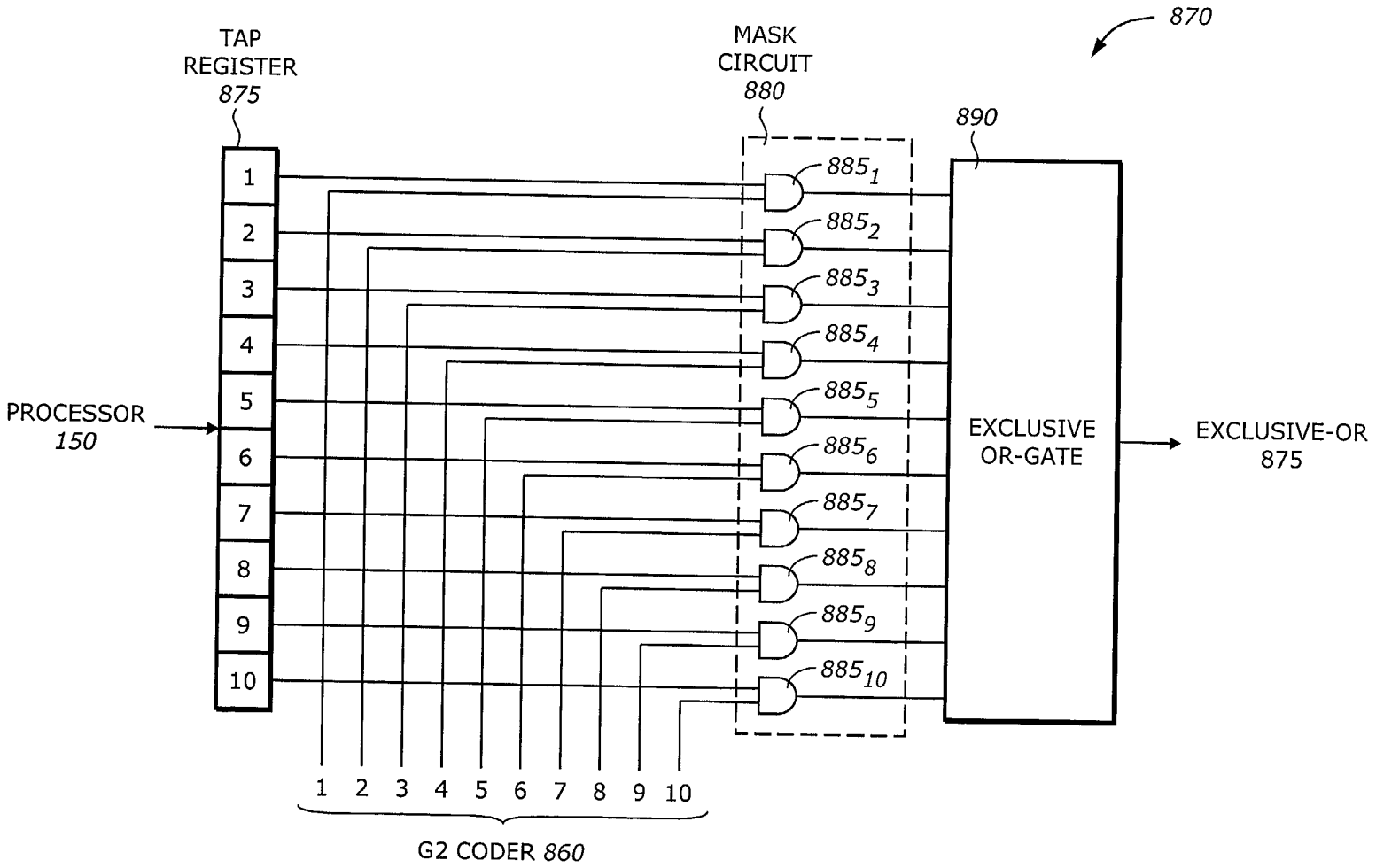
870
TAP REGISTER 875
MASK CIRCUIT 880
890
PROCESSOR 150
1
2
3
4
5
6
7
8
9
10
885_1
885_2
885_3
885_4
885_5
885_6
885_7
885_8
885_9
885_{10}
EXCLUSIVE OR-GATE
EXCLUSIVE-OR 875
1 2 3 4 5 6 7 8 9 10
G2 CODER 860

FIG. 8C

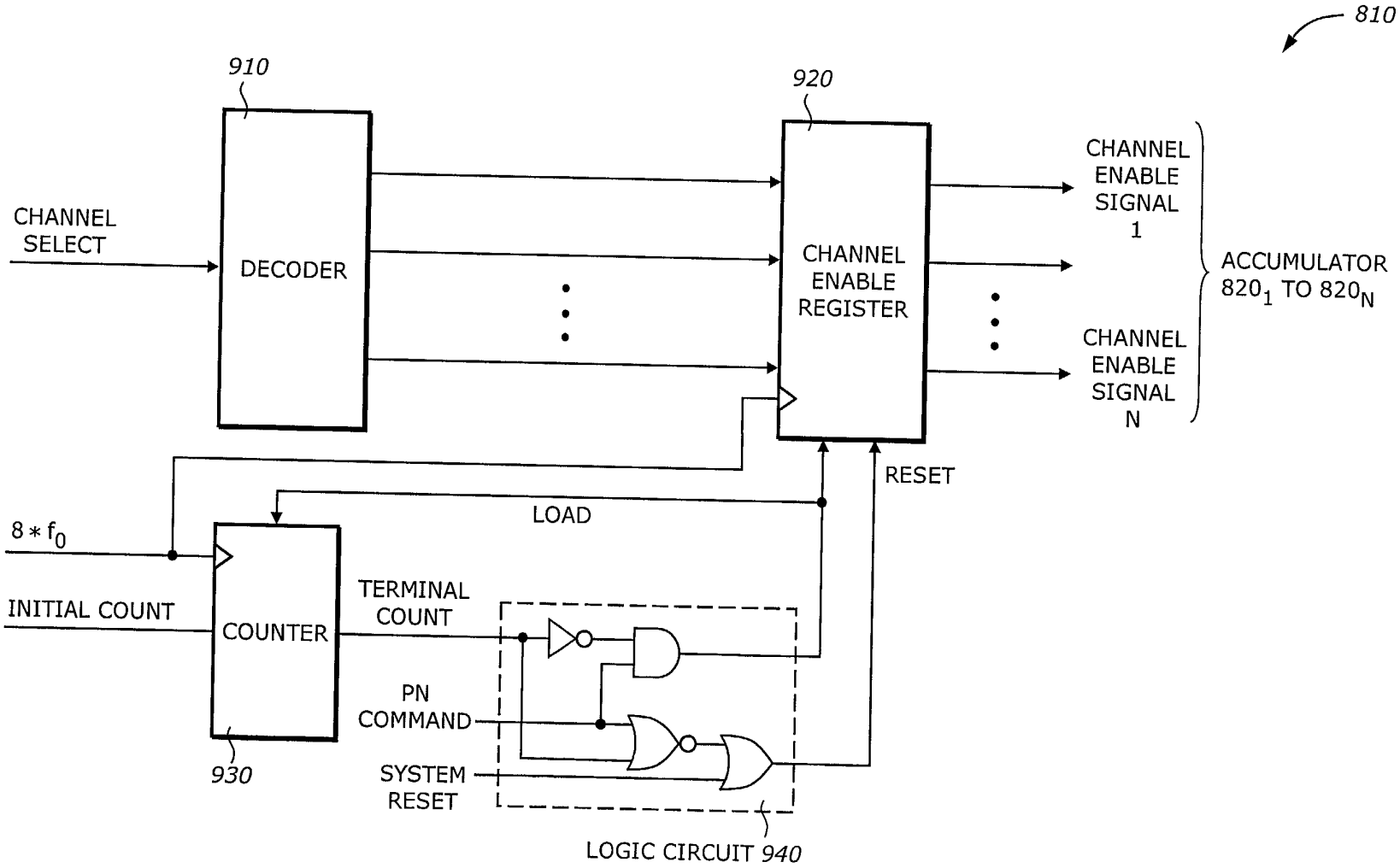
810
910
920
CHANNEL SELECT
DECODER
CHANNEL ENABLE REGISTER
CHANNEL ENABLE SIGNAL 1
CHANNEL ENABLE SIGNAL N
ACCUMULATOR 820$_1$ TO 820$_N$
RESET
LOAD
8 * f$_0$
INITIAL COUNT
COUNTER
TERMINAL COUNT
PN COMMAND
SYSTEM RESET
930
LOGIC CIRCUIT 940

FIG. 9

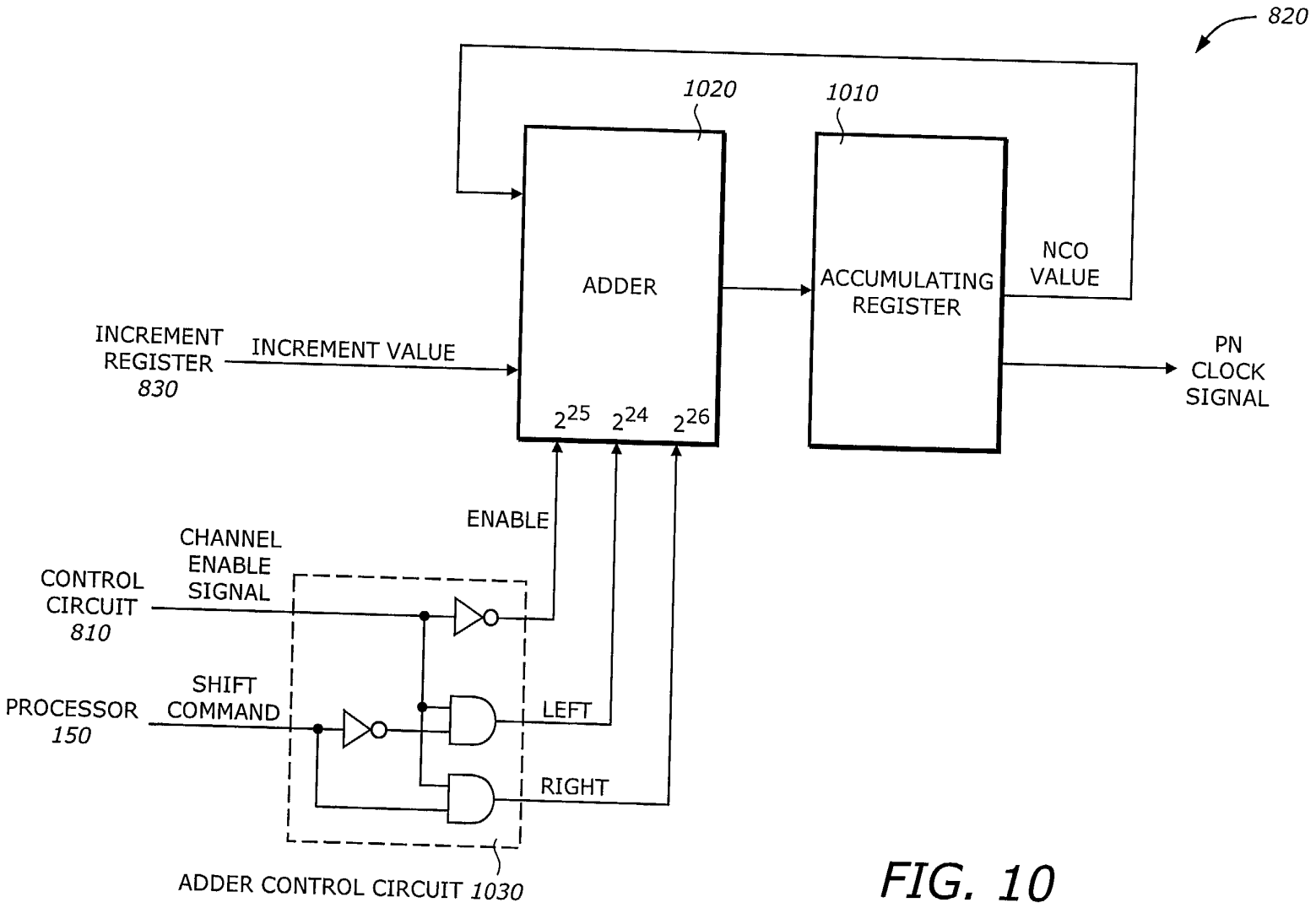
820
1020
1010
ADDER
ACCUMULATING REGISTER
NCO VALUE
INCREMENT REGISTER 830
INCREMENT VALUE
PN CLOCK SIGNAL
2^{25} 2^{24} 2^{26}
ENABLE
CHANNEL ENABLE SIGNAL
CONTROL CIRCUIT 810
SHIFT COMMAND
PROCESSOR 150
LEFT
RIGHT
ADDER CONTROL CIRCUIT 1030

FIG. 10

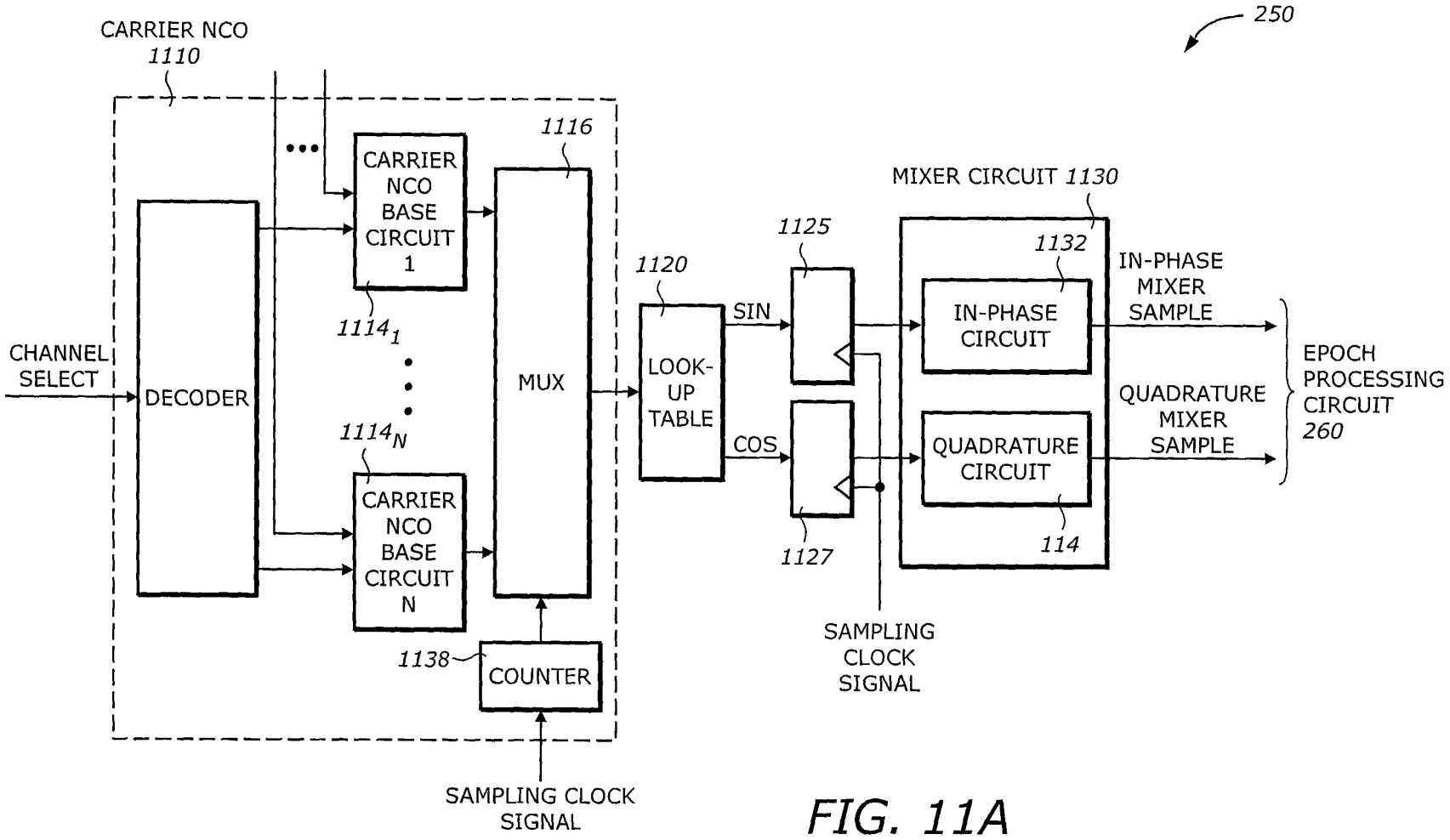

FIG. 11A

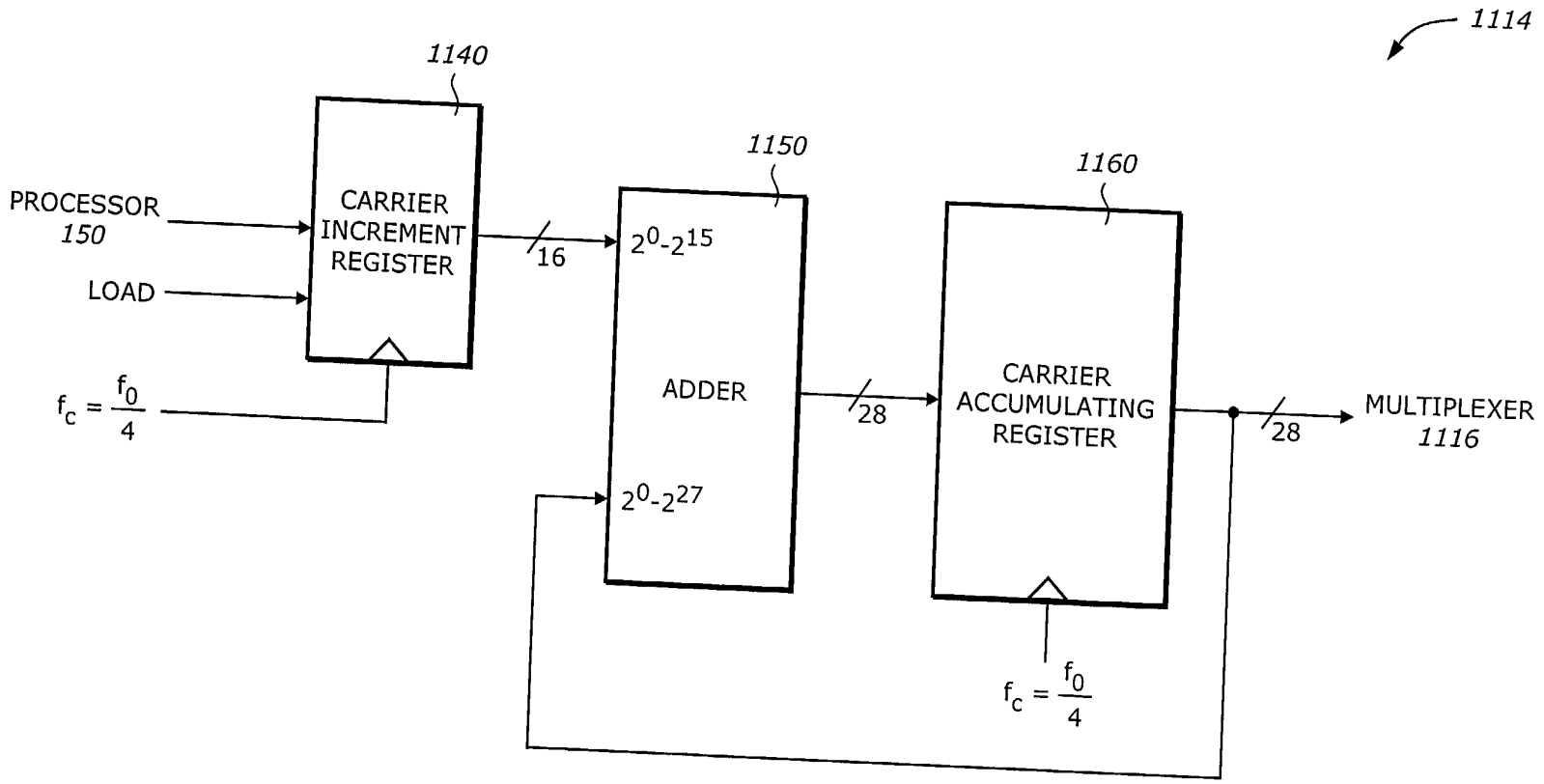
1114
1140
1150
1160
PROCESSOR
150
LOAD
CARRIER
INCREMENT
REGISTER
16
2^0-2^{15}
ADDER
2^0-2^{27}
28
CARRIER
ACCUMULATING
REGISTER
28
MULTIPLEXER
1116
$f_c = \frac{f_0}{4}$
$f_c = \frac{f_0}{4}$

FIG. 11B

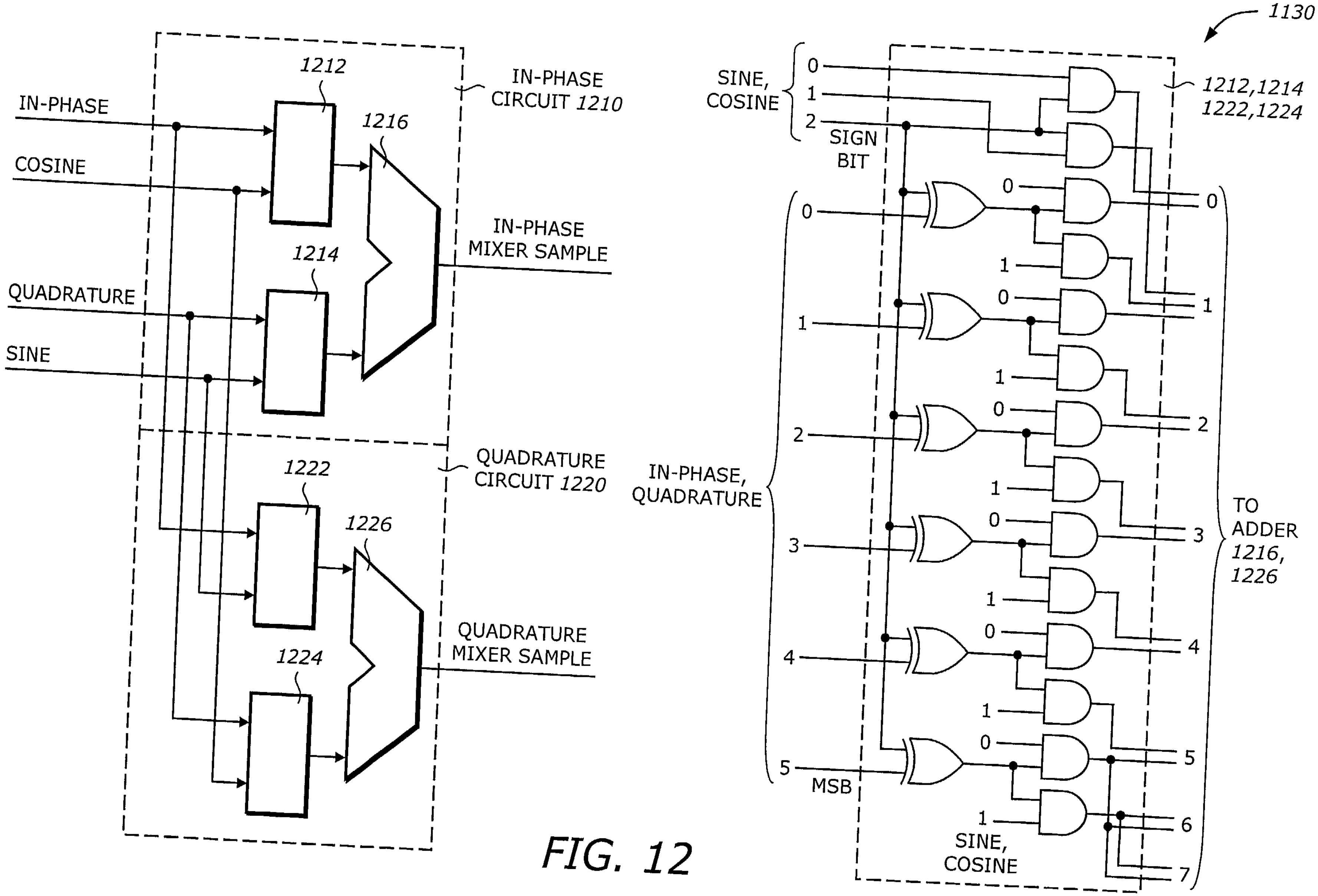
IN-PHASE
COSINE
QUADRATURE
SINE
1212
1214
1216
1222
1224
1226
IN-PHASE CIRCUIT 1210
IN-PHASE MIXER SAMPLE
QUADRATURE CIRCUIT 1220
QUADRATURE MIXER SAMPLE
1130
SINE, COSINE
0
1
2
SIGN BIT
1212,1214 1222,1224
IN-PHASE, QUADRATURE
0
1
2
3
4
5
MSB
SINE, COSINE
TO ADDER 1216, 1226
0
1
2
3
4
5
6
7

FIG. 12

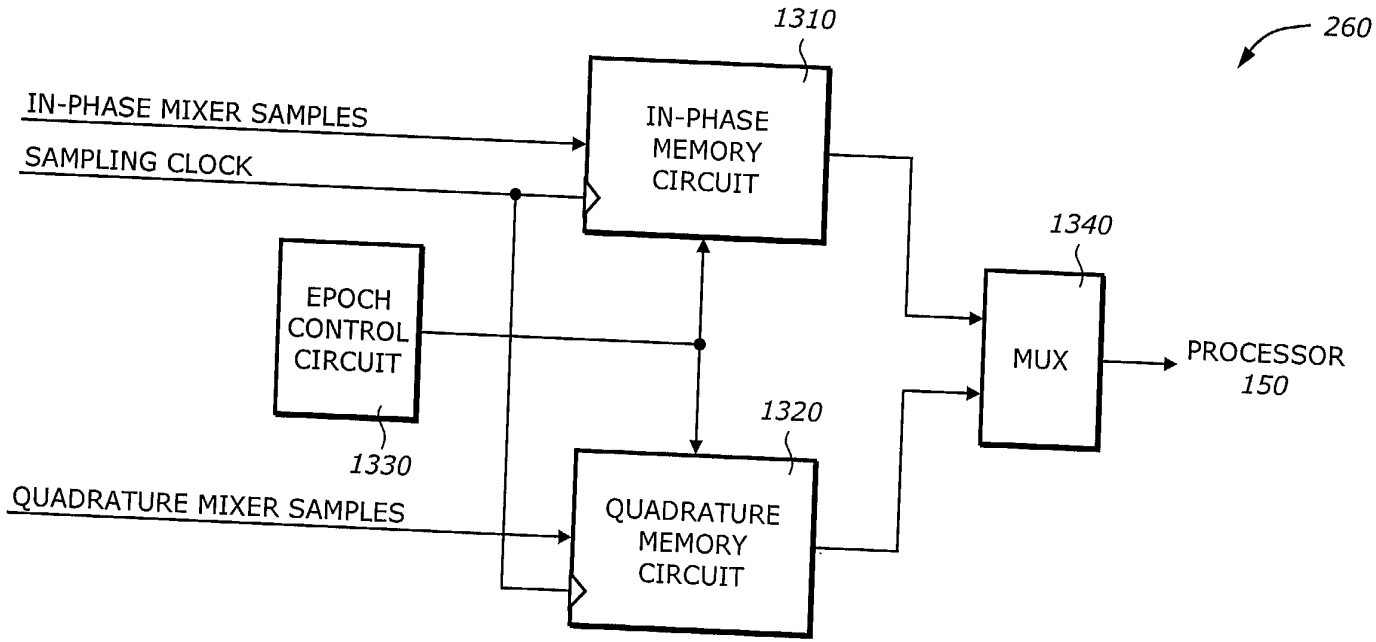

FIG. 13

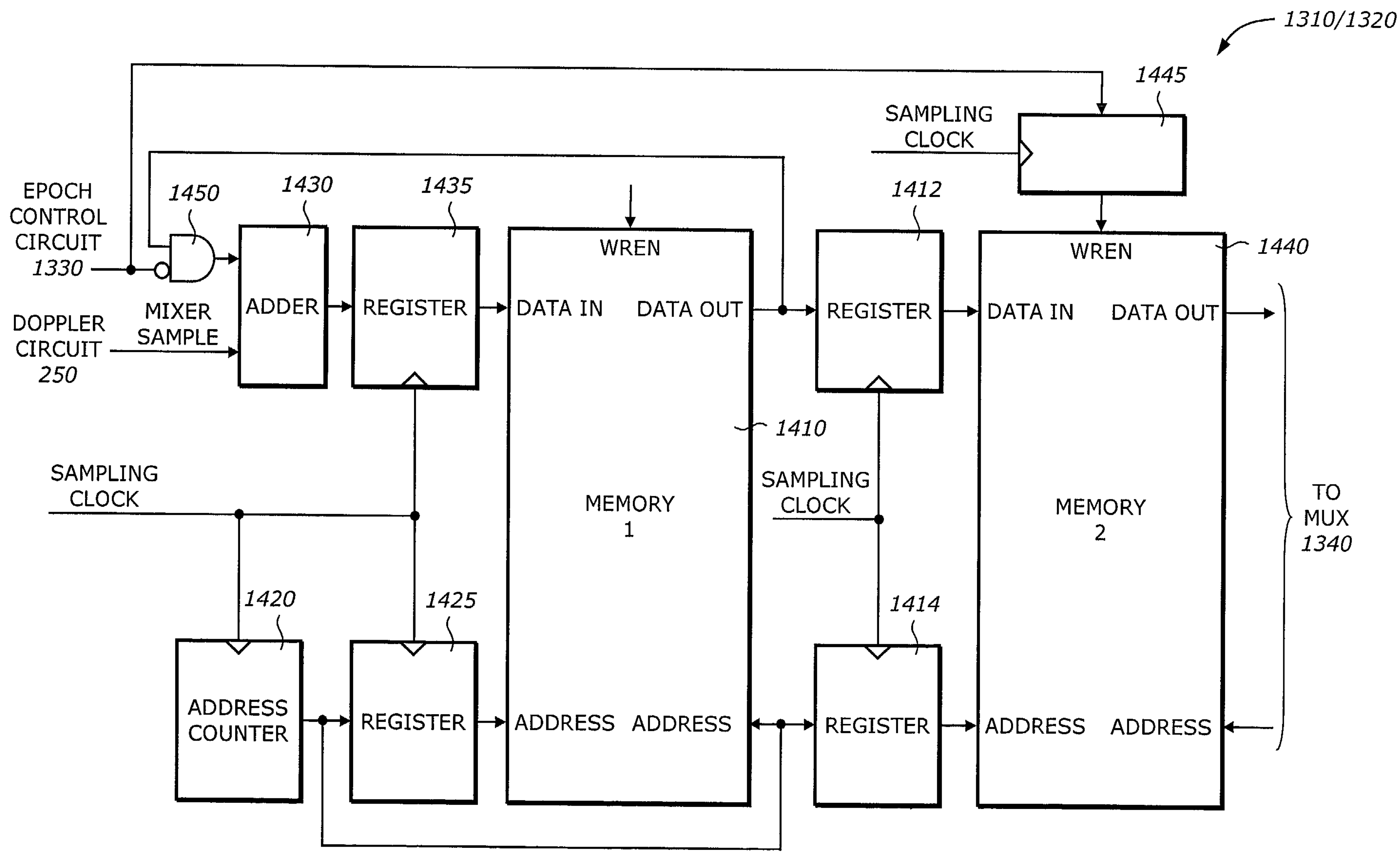

FIG. 14